10

BIRZEIT UNIVERSITY

Faculty of Engineering and Technology
Electrical and Computer Engineering Departmen
Advanced Digital Design ENCS533

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A. Write a behavioral description for the MUX4x1.
B. Write a testbench for the MUX4x1.

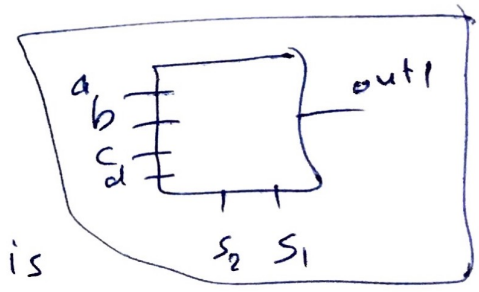
A.

```
Entity mux4_1 IS
 PORT ( a, b, c, d, s1, s2: IN STD_LOGIC;
        out1 : OUT STD_LOGIC);
End entity mux4_1;

architecture simple of mux4_1 is
 Begin
   out1 <= a when s1='0' and s2='0'
      Else b when s1='1' and s2='0'
      Else c when s1='0' and s2='1'
      Else d when s1='1' and s2='1';
End architecture simple;
```

s2	s1
0	0
0	1
1	0
1	1

5



B.

```
Entity test_mux is
 End Entity test_mux;

architecture test of test_mux is
 signal a, b, c, d, s1, s2, out1 : STD_LOGIC;
 Begin
   s1 <= '0' , '1' after 20 ns, '0' after 40 ns;
   s2 <= '0' , '1' after 30 ns; '0' after 60 ns;
   a <= '0' , '1' after 50 ns, '0' after ...

Entity work.mux4_1 (simple) port map (a,b,c,d,s1,s2,out1);
```

5

```
b <= '0',
     '1' after 10 ns;

c <= '0',
     '1' after 30 ns;

d <= '0',
     '1' after 60ns;

End architecture test;
```

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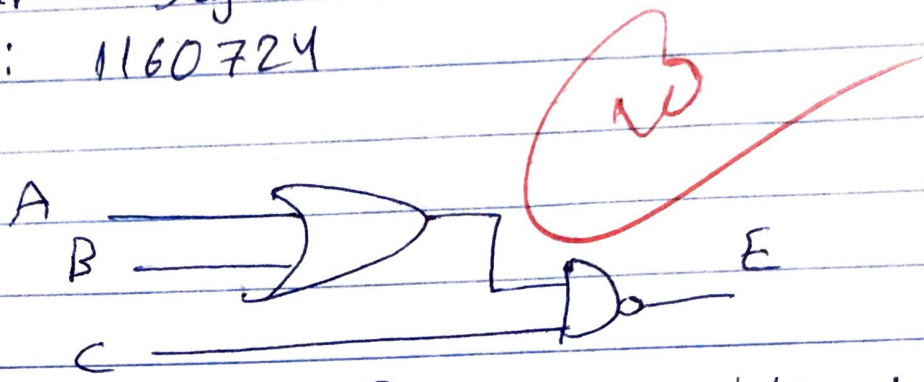

find when E is sensitive to B.

$E = f(A, B, C) = ((A+B).C)'$

$= (A+B)' + C'$

$= A'B' + C'$

$\frac{dE}{dB} = f(B=0) \oplus f(B=1)$

$= (A' + C') \oplus C' = 1$

$A' + C' = 1$ or $C' = 1$

but not both

A	C	A'	C'	A' + C'	(A' + C') ⊕ C'
0	0	1	1	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	1	0	0	0	0

E is sensitive to B when $\overline{AC} = 01$

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	00	01	11	10
a	(a), 0	b, –	–, –	d, –
b	a, –	(b), 1	(b), 1	c, –
c	b, –	–, –	b, –	(c), 0
d	c, –	(d), 1	c, –	(d), 1

	00	01	11	10
a	0	X	X	X
b	X	1	1	X
c	X	X	1	0
d	X	1	1	1

Y